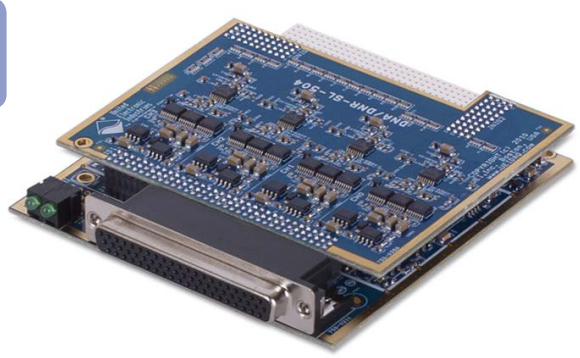
DNA/DNR-SL-504

4-Port Synchronous Serial Interface

- DNA-SL-504 for use with "Cube" I/O chassis
- DNR-SL-504 for use with RACKtangle™ I/O chassis
- 4 independently configurable ports
- Each port software-configurable as RS-232 or RS-485/422/423
- Max speed of 256 Kbaud for RS-232 and 4 Mbaud for RS-485/422
- Async, HDLC/SDLC protocol support
- TX/RX Synchronization signal on each channel
- 350 port-to-port isolation; 15kV ESD

10-Year Availability Guarantee



General Description

The DNA/DNR-SL-504 are 4-port serial communications interfaces for Cube/RACKtangle I/O chassis respectively. Each port is independently configurable as RS-232, RS-485, RS-422/423 as well as set for synchronous or asynchronous communications. Each port is fully isolated from the other three ports as well as from the Cube or RACKtangle chassis. The board is an ideal interface to a wide variety of serial based data acquisition and control interfaces as well as general purpose serial I/O.

The DNx-SL-504 is based on the Zilog Z16C32 serial controller chip and supports most popular synchronous serial protocols including HDLC and SDLC. The HDLC/SDLC interface provides full access to the serial frames. User code can then determine how to handle retry or protocol corrections. The RS-485/422 implementation provides transmit and receive data, synch and clock interfaces. The RS-232 configuration also supports CTS signals. The maximum transfer rate in RS-485/422 and RS-232 modes are 4 Megabaud and 600 kbaud respectively.

The DNA/DNR-SL-504 support standard asynchronous serial transfer rates up to 2 Mbaud in RS-485 mode or up to 256 kbaud in RS-232 mode. It also supports communications at 12, 12.5 and 50 kbaud with better than 0.1% data rate accuracy. The UART supports 5, 6, 7, or 8 data bits, plus optional even or odd parity. The transmitters will also supply 1, 2, or fractional stop bits per character and can provide a break output at any time. The following section provides a bit more detail on the various modes supported and how they are implemented and accessed.

Supported modes:

a. HDLC with synchronous and asynchronous framing
b. Asynchronous and synchronous serial (byte-oriented, like SL-508), parity: none/even/odd/mark/space
c. Raw mode (user-controlled FIFO-based synchronous

HDLC

a. Frame data programming – i.e. address and control fields as well as flow control and sequence numbering are at the user discretion – no layer 3 protocol support
b. Frame size for up to 4096 bytes (0x7E flags – data – 0x7E flag)
c. Received frames can be filtered by address and/or broadcast address
d. Transmit frames can have FCS field with CRC16 or CRC32 populated automatically (CRC type is selectable), receive frames are checked against received CRC
e. Frame statistics is accumulated and available (number of success/failures/aborted/received/transmitted frames, overruns/underruns)
f. No flow control implemented
g. Preamble length and preamble is selectable: 16, 32 or 64 bits; all zeroes, all flags, interleaved 1 and 0s or all 1s
h. On underrun sends 7/15 bit abort code, optionally CRC and flag to close the frame normally
i. An idle mode transmitter can stream continuous flags, 0/1s, marks/spaces or alternate them
j. Frame size is always a multiple of 8-bit bytes

Technical Specifications:

Port Specifications	
Number ports	4, independently configurable
UART type	Zilog Z16C32
Interface types	RS-232, RS-422/423, RS-485
Protocols	Async, HDLC, SDLC
FIFOs	32byte, input and output (per port)
Baud rate generator	Programmable, 1.2 kbaud to 4 Mbaud
RS-232 specifications	
RS-232 Asynchronous	256 kbaud
RS-232 Synchronous	600 kbaud
RS-232 Signals	Tx, TxCLK Out, Rx, RxCLK In, CTS, Sync, DCD
RS-485/422 specifications	
RS-485/422 Async	1 Mbaud
RS-485/422 Synchronous	4 Mbaud
RS-485/422 Signals	Tx+, Tx-, TxCLK+, TxCLK-, RX+, RX-, RxCLK+, RxCLK- CTS+. CTS-, DCD+, DCD-
General Specifications	
Isolation	350 V port to port;
ESD protection	15 kV
Power Consumption	2-5W (RS-485 mode with max current drive)
Operating Temperature	Tested -40 to +65 °C
Operating Humidity	0 - 95%, non-condensing
Vibration *IEC 60068-2-6* *IEC 60068-2-64*	5 g, 10-500 Hz, sinusoidal 5 g (rms), 10-500 Hz, broad-band random
Shock *IEC 60068-2-27*	50 g, 3 ms half sine, 18 shocks @ 6 orientations 30 g, 11 ms half sine, 18 shocks @ 6 orientations
MTBF	290,000 hours

Interface modes:

a. RS-232, RS-485, RS-422/423 w/termination
b. Encoding: NRZ and inverted, NRZI mark or space, biphase mark or space, biphase-level or differential
c. Asynchronous and synchronous modes (in synchronous both data and clock lines are used)
d. Baud rate: RS-232 up to 256k, balanced up to 4Mbit/s
e. Use automatically/ignore/CTS and DCD lines
f. Receive/transmit clocks can be recovered from DPLL or taken from RxC or TxC line (proper encoding mode must be used).

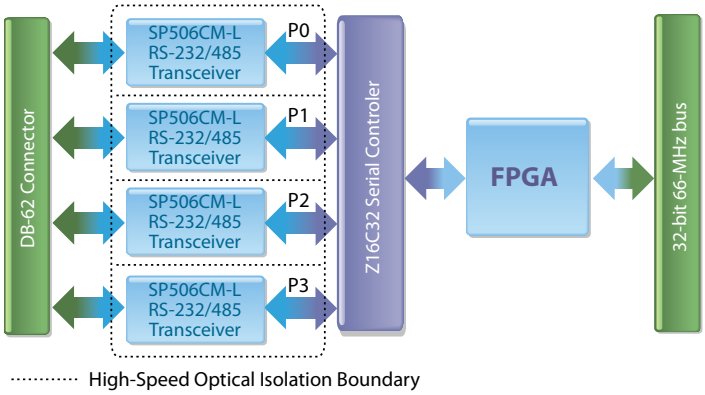
The DNA/DNR-SL-504 are compatible with RS-422 point to point or RS-485 network applications. The ports are based on the Exar SP506CM-L series drivers and provide a wide variety of I/O configurations.

The DNA/DNR-SL-504 is supported by the UEIDAQ Framework providing a simple and complete software interface to all popular Windows programming languages and DAQ applications. Support is also provided for all popular "non-Windows" operating systems including Linux, VXworks, QNX, RTX, INtime and more.

Connection Options:

Cable/STP	Description
DNA-STP-62	Break-out panel that breaks each serial port out to screw terminals
DNA-CBL-62	62 conductor cable connects directly to OEM equipment or to the DNA-STP-62 screw terminal panel

Block Diagram



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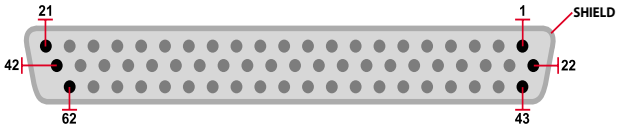

Pin	*signal*	*Pin*	*signal*	*Pin*	*signal*
1	RESERVED01	22	GND-CH0	43	RxC(a)-0
2	TxC(b)-0	23	TxC(a)-0	44	RxC(b)-0
3	DCD(a)-0	24	DCD(b)-0	45	GND-CH0
4	RxD(b)-0	25	RxD(a)-0	46	RESERVED11
5	TxD(b)-0	26	TxD(a)-0	47	CTS(b)-0
6	GND-CH1	27	CTS(a)-0	48	RESERVED17
7	RxC(b)-1	28	RxC(a)-1	49	DCD(b)-1
8	TxC(b)-1	29	TxC(a)-1	50	DCD(a)-1
9	RxD(b)-1	30	RxD(a)-1	51	GND-CH1
10	TxD(b)-1	31	TxD(a)-1	52	CTS(a)-1
11	RESERVED33	32	CTS(b)-1	53	RxC(a)-2
12	TxC(b)-2	33	TxC(a)-2	54	RxC(b)-2
13	DCD(b)-2	34	GND-CH2	55	GND-CH2
14	RxD(b)-2	35	RxD(a)-2	56	DCD(a)-2
15	TxD(b)-2	36	TxD(a)-2	57	CTS(b)-2
16	GND-CH3	37	CTS(a)-2	58	RESERVED49
17	RxC(b)-3	38	RxC(a)-3	59	DCD(b)-3
18	TxC(b)-3	39	TxC(a)-3	60	RESERVED55
19	DCD(a)-3	40	GND-CH3	61	RxD(a)-3
20	TxD(b)-3	41	TxD(a)-3	62	RxD(b)-3
21	CTS(a)-3	42	CTS(b)-3		

Notes:

1. No user connections to the Reserved pins are allowed.