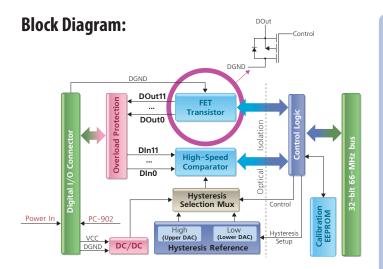


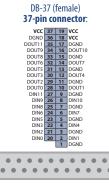
General Description:

The DNA-DIO-406 and DNR-DIO-406 are 24 channel digital I/O boards compatible with UEI's "Cube" and RACKtangle I/O chassis respectively. The DNA/DNR-DIO-406 is packed with a number of unique features: as many as 24 DIO lines 350V RMS isolated as a group, pre-configured with 12 inputs and 12 outputs, powerful user-programmable hysteresis that improves noise immunity of the digital input signals. The unit requires either external power (3.3-36VDC) or the installation of the DNA-PC-912, 24VDC power source. The DNA-DIO-406 layer is capable of continuously sinking 1 Amp per channel on all outputs, and provides readings on all inputs with available change-of-state detection.

Outputs feature low impedance FET transistors that are configured in a "lowside" mode (logic 1 connects output to the DGND via FET, logic low keeps output floating), user loads should be connected between VCC and the output. This layer is also capable of driving solenoids - output FET transistor has a reverse protection diode, for extra protection it is recommended to add a reverse diode directly at the inductive load. DNA-DIO-406 has a maximum update rate of 100kS/s. The DNA/ DNR-DIO-406 boards are an ideal digital I/O interface in a wide vareity of PC based data acquisition, data logging and industrial control applications.



Pinout Diagrams:



Note: Connect external power source to VCC pins. All VCC and at least 3 **DGND** pins should be used to supply external power.

Digital Lines	12 inputs; 12 outputs (sink)					
Logic Level	3.3-36V; rated for 3.3V, 5V, 12V, 24V, 36V					
Input Current	360µA max					
Input FIFO	512 samples					
Input Protection	±40V over/under voltage, 3 kV ESD					
Default Hysteresis Values	Lower Limit: 0; Upper Limit: 300					
Input High Voltage: (with default hysteresis)	@3.3V	@5V	@12V	@24V	@36V	
	1.6V	2.7V	7.5V	12V	17V	
Input Low Voltage: (with default hysteresis)	@3.3V	@5V	@12V	@24V	@36V	
	1.5V	1.8	2.0V	3.0V	12.5V	
Output Drive Capacity	continuous: 1000 mA per channel maximum peak: 1500mA per channel					
Output FIFO	1024 samples					
Output High Voltage:	Output Floating					
Output Low Voltage	1.5 Volt max at 1 Amp					
Output Protection	2 Amp, slow-blow fuse (one per channel)					
Internal Sampling Rate	1 MHz					
I/O Throughput Rate	100kHz m	100kHz max				
Power Requirements (VCC)	3.3-36V (24V nominal) - external source or DNA-PC-912 internally					
Power Consumption	0.7W (no load) @ 3.3V VCC; 1.8W (no load) @ 36V VCC; ~ 0.22W/per output at 1000mA load					
Physical Dimensions	3.875″ x 3	3.875" x 3.875" (98 x 98 mm)				
Operating Temp. Range	Tested -40	Tested -40 to +85 °C				
Operating Humidity	0 - 95%, non-condensing					
Isolation	350Vrms					

Connection Options:

Cable	Screw Terminal Panel	Description	
DNA-CBL-37S	DNA-STP-37	Shielded cable connection to 37-way terminal panel.	
DNA-CBL-37	DNA-STP-37	Ribbon cable connection to 37-way terminal panel.	
United Electronic In	dustries, Inc.	1	http://www.ueidag.com

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Hysteresis Setup:

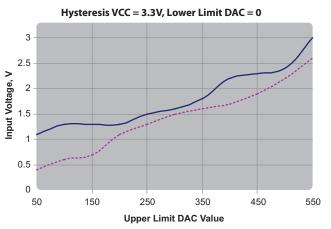
Hysteresis is a very powerful feature that improves noise immunity on the digital inputs in industrial environments. Hysteresis on the DNA-DIO-404 is implemented as follows:

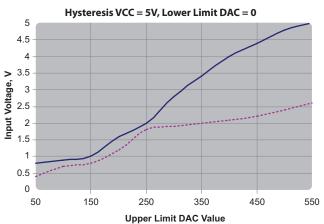
Two user programmable digital-to-analog converters are used to set upper and lower limits for the hysteresis function. These D/A converters are referred to as Lower limit DAC and Upper limit DAC. DAC outputs are connected to the high speed comparators via a multiplexer.

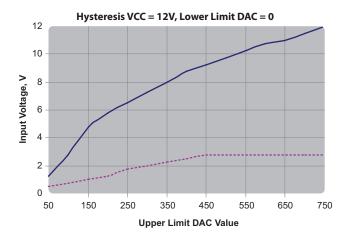
- All inputs initially are read from the comparators while comparing with the Lower DAC
- Another read is performed while comparators are connected to the Upper limit DAC
- If the digital input values from both reads are the same, the input signal state is assigned to the last read value
- If input values from Lower DAC and Upper DAC read are different, the input signal state remains unchanged
- This process repeats itself 1000000 times per second

Set the hysteresis values by programming the Lower and Upper DACs. Below is a set of graphs to set hysteresis for all rated voltages, and also the function in the PowerDNA API which automatically selects the closest values of the Lower and Upper DACs based on user - requested hysteresis settings. Upper and Lower DACs may be programmed with an arbitrary integer number from 0 to 1023. The value of the Upper DAC should always be greater than LowerDAC by at least 50. Actual DAC values should be selected based on user requirements from the graphs below.

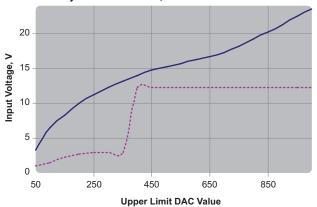
On all graphs below, the blue solid line represents voltage required on the input for the low-to-high transition, and pink dashed line represent voltage required on the input line for the high-to-low transition.

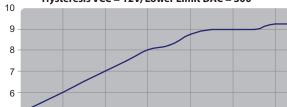




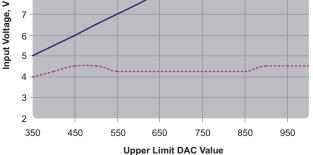








Hysteresis VCC = 12V, Lower Limit DAC = 300



Hysteresis VCC = 24V, Lower Limit DAC = 200

