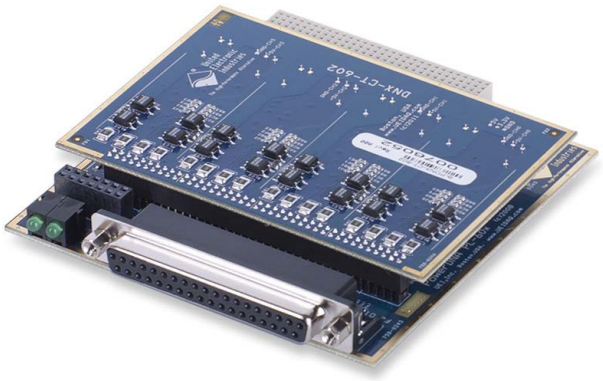
DNA/DNR-CT-602

High Speed Differential Counter/Timer Board

10-Year Availability Guarantee

- DNA-CT-602 for use with "Cube" data acquisition & logging chassis
- DNR-CT-602 for use with RACKtangle™ I/O chassis
- 4 independent 32-bit counter/timer units;
- Fully differential inputs/outputs at RS-422/485 logic levels
- 8 Counting modes
- 32-bit prescaler per channel;
- Internal (66 MHz) or external (max 16.5 MHz) timebases
- 256 x 32-bit Input FIFO and 256 x 32-bit Output FIFO on each counter
- Debouncing/glitch removal on external clock and gate inputs



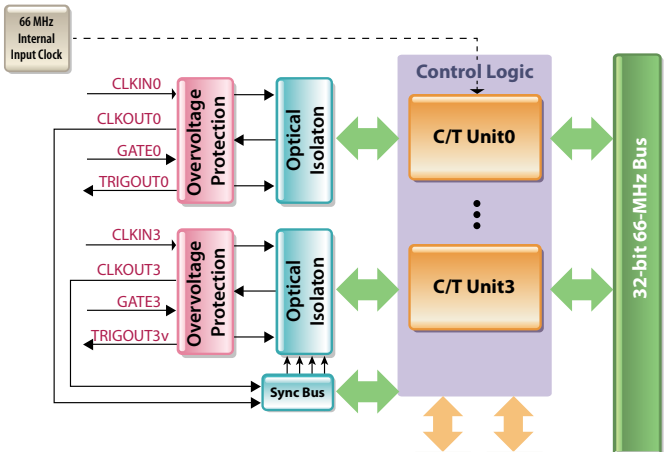
Supports **UEIDaq Framework** Data Acquisition Software Library for Windows. Linux, VXworks and QNX drivers available. Visit our website for more details.

General Description

The DNA-CT-602 and DNR-CT-602 are differential counter/timer interfaces for UEI's "Cube" and RACKtangle I/O chassis respectively. The DNA/DNR versions are electrically identical and provide four independent 32-bit channels, each one having overvoltage protection and opto-isolation. They perform up/down counting in a number of flexible modes using values from a Load Register and two Compare Registers. They can act as an event counter, perform width/period measurements and run in quadrature-encoder mode where the user sets the direction of the counting. For output modes, the layer offers 1-shot and Universal PWM operation. It also provides edge detection on the ClockIn and Gate pins. The DNx-CT-602 is software compatible with the DNx-CT-601 except for the additional commands which configure and control the Trigger Output pins. The DNx-CT-602 provides the following 8 counting modes which will accommodate most data acquisition and data logging requirements:

- Timer
- PWM generator
- Continuously updated PWM generator (buffered)
- Bin counter (number of pulses in specified time interval)
- Pulse width
- Pulse period (2^{32} periods max)
- Quadrature encoder
- Timebase operation

Block Diagram



Notes:
1. Any counter input may be internally connected to the 66 MHz internal bus clock.
2. Any counter output may be internally connected to any inter-board synch bus signal.

Technical Specifications:

Number of counter/timer units	4
Resolution	32 bits
Prescaler (per channel)	1 (32 bits)
Maximum frequency	16.5 MHz for external input clock; 66 MHz for internal input clock; 33 MHz for outputs
Minimum frequency	no low limits
On-board FIFOs, per counter	Input: 256 x 32; Output: 256 x 32
Minimum pulse width	15.15 nS
Minimum period	30.30 nS
Measurement resolution	15.15 nS (standard mode) 7.5 nS (2X mode)
Internal 66 MHz time base (from backplane clock signal)	Initial accuracy: ±10 ppm Temp drift: ±15 ppm over full temp range Time drift: ±5 ppm year one, then lower
Debouncer circuit size	16 bits (on GATE and CLKIN)
Compare registers per counter	2
External gates per counter	1, programmable polarity
External triggers per counter	1 (shared with Gate), edge sensitive, programmable polarity
Protection	7 kV ESD, 350V isolation
Input High / Low voltage	RS-422/485 compatible
Electrical Isolation	350 Vrms, chan-chan and chan-chassis
Output High / Low voltage	RS-422/485 compatible
Input/output buffer chip	LTC1686 or equivalent
Power consumption	2W
Operating range	Tested -40 to +85 °C
Humidity range	0 - 95%, noncondensing
Vibration *IEC 60068-2-6* *IEC 60068-2-64*	5 g, 10-500 Hz, sinusoidal 5 g (rms), 10-500 Hz, broad-band random
Shock *IEC 60068-2-27*	50 g, 3 ms half sine, 18 shocks @ 6 orientations 30 g, 11 ms half sine, 18 shocks @ 6 orientations

Connection Options:

Cable	Terminal Panel	Description
DNA-CBL-37	DNA-STP-37	DNA-CBL-37 3 foot ribbon cable connects directly to the DNA-STP-37 Screw Terminal Panel.
DNA-CBL-37S	DNA-STP-37	DNA-CBL-37S 3 foot shielded cable connects directly to the DNA-STP-37 Screw Terminal Panel.

Pinout Diagram:

DB-37 (female) connector