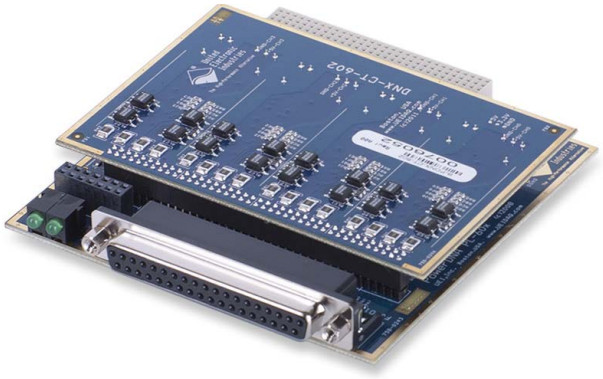
DNA/DNR-CT-602-804

Differential Synchronous Serial I/O board

10-Year Availability Guarantee

- DNA-CT-602 for use with "Cube" data acquisition & logging chassis
- DNR-CT-602 for use with RACKtangle™ I/O chassis
- 4 independent channels, each can be configured as a General purpose synchronous serial port (Tx, Rx, Clk, Trig, Ack)
- Fully differential inputs/outputs at RS-422/485 logic levels
- Supports SSI communications protocol in serial mode
- Programmable data word and frame synch length in serial mode.



General Description

The DNA-CT-602-804 and DNR-CT-602-804 are high performance multipurpose interfaces for UEI's "Cube" and RACKtangle I/O chassis respectively. The DNA/DNR versions are electrically identical and provide four independent channels, each having over voltage protection and opto-isolation. The 602-804 differs from the standard DNx-CT-602 in that it also implements a synchronous serial interface. Any of the 4 channels can be configured as independent communications ports.

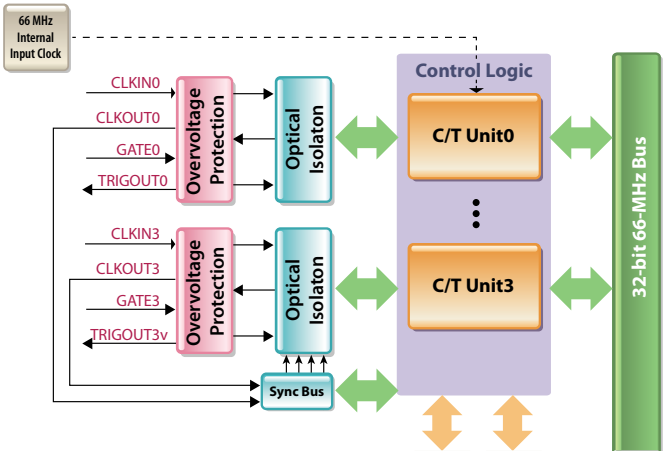
Software included with the DNx-CT-602-804 provides a comprehensive yet easy to use API supporting all popular Windows programming languages as well as programmers using Linux and most real-time operating systems including QNX, RTX, VXworks and more. Finally, the UEIDAQ Framework supplies complete support for those creating applications in data acquisition software packages such as LabVIEW, MATLAB/Simulink, or any application which supports ActiveX or OPC servers.

Synchronous Serial Mode

UEI offers a broad range of serial I/O layers however none of them is providing support for the so-called "Clock/Data/Sync" legacy synchronous protocols. These special protocols as well as the standard SSI protocol have been addressed by adding special mode of the operation to the CT-602-804 counter-timer board. This mode called Generic Synchronous Serial Protocol (or GSSP) and can be configured to support different variations of "Clock/Data/Sync" from multiple vendors. The following bullet items describe the various features of the DNx-CT-602-804 in its Synchronous Serial Mode.

- Four independent channels, GSSP mode can be enabled individually on each channel, while counter functionality of other CT-602 is unaffected. (In some modes, a channel is dedicated to generating the baud rate clock.)
- Electrical specifications: RS-485/422 complaint
- Data rates: 300bps - 16Mbps (maximum sustained rate for the layer is 2MB/sec, 4MB/sec aggregate for all boards in a single DNA/DNR chassis)
- Data word length 3-32 bits
- Clock source: internal (with 0.1% or better accuracy) or external, 1 TX/RX bit per clock
- FIFO 1024x32 for TX and RX with watermark, Asynchronous event/interrupt generated upon FIFO full
- Special mode of the operation for the TX FIFO with dynamically variable word length
- Pin utilization
  - Transmission:
    - » ClkIn - input SyncClock from UUT . Transmission clock could be also derived internally from the PLL with post-divide on prescaler
    - » ClkOut - data.
    - » Gate - transmission can be triggered either by the software or by this line, edge or level is software selectable. Following modes supported:
      - transmit one frame per trigger
      - transmit until the FIFO is not empty
      - transmit while TrigIn is asserted (always transmit full words)
      - transmit until bit special "stop" bit is set (full 32-bit transmission still supported)
    - » TrigOut - produces FrameSync when external baud clock is applied to ClkIn or SyncClock when baud rate is derived internally
  - Reception:
    - » ClkOut - generate baud clock for UUT transmissions.
    - » ClkIn - data from UUT
    - » Gate - FrameSync from UUT.
- FrameSync length is programmable (1 bit/N bits/Word/Frame)
- FrameSync phase relatively to SyncClock can be programmed in 15.15ns increments
- Frame length can be set between 1 and 1024 bytes.
- DataIn/DataOut can be encoded/decoded using NRZ and NRZI.
- DataIn/DataOut signal may be pre-/post- inverted.
- Data edge can be adjusted in 15.15nS increments relative to the SyncClock

Block Diagram



Notes:
1. Any counter input may be internally connected to the 66 MHz internal bus clock.
2. Any counter output may be internally connected to any inter-board synch bus signal.

Technical Specifications:

COUNTER/TIMER Functions	
Number of counter/timer units	4
Resolution	32 bits
Prescaler (per channel)	1 (32 bits)
Maximum frequency	16.5 MHz for external input clock; 66 MHz for internal input clock; 33 MHz for outputs
Minimum frequency	no low limits
On-board FIFOs, per counter	Input: 1024 x 32; Output: 1024 x 32
Minimum pulse width	15.15 nS
Minimum period	30.30 nS
Measurement resolution	15.15 nS (standard mode) 7.5 nS (2X mode)
Debouncer circuit size	16 bits (on GATE and CLKIN)
Compare registers per counter	2
External gates per counter	1, programmable polarity
External triggers per counter	1 (shared with Gate), edge sensitive, programmable polarity
SYNCHRONOUS SERIAL Ports	
Baud Rate	300 to 16 Megabaud (2 Mb sustained, 4 Mb max per DNA/DNR chassis
Baud Rates available	User selectable 0.1% accuracy or better
Data Word Length	3 - 32 bits
FIFO (on each channel)	Input: 1024 word, Output: 1024 word
FrameSync phase control	Programmable in 15.15 nS increments
GENERAL SPECIFICATIONS	
Protection	7 kV ESD, 350V isolation
Input High / Low voltage	RS-422/485 compatible
Electrical Isolation	350 Vrms, chan-chan and chan-chassis
Output High / Low voltage	RS-422/485 compatible
Input/output buffer chip	LTC1686 or equivalent
Power consumption	2W
Operating range	Tested -40 to +85 °C
Humidity range	0 - 95%, noncondensing
Vibration *IEC 60068-2-6* *IEC 60068-2-64*	5 g, 10-500 Hz, sinusoidal 5 g (rms), 10-500 Hz, broad-band random
Shock *IEC 60068-2-27*	50 g, 3 ms half sine, 18 shocks @ 6 orientations 30 g, 11 ms half sine, 18 shocks @ 6 orientations

Pinout Diagram (counter/timer):

Please refer to the following page for serial connections.

DB-37 (female) connector

CLKOUT(0)+	1	20	CLKOUT(0)-
GATE(0)+	2	21	GATE(0)-
TRIGOUT(0)+	3	22	TRIGOUT(0)-
CLKIN(0)+	4	23	CLKIN(0)-
GND(0)	5	24	GND(1)
CLKOUT(1)+	6	25	CLKOUT(1)-
GATE(1)+	7	26	GATE(1)-
TRIGOUT(1)+	8	27	TRIGOUT(1)-
CLKIN(1)+	9	28	CLKIN(1)-
CLKOUT(2)+	10	29	CLKOUT(2)-
GATE(2)+	11	30	GATE(2)-
TRIGOUT(2)+	12	31	TRIGOUT(2)-
CLKIN(2)+	13	32	CLKIN(2)-
GND(2)	14	33	GND(3)
CLKOUT(3)+	15	34	CLKOUT(3)-
GATE(3)+	16	35	GATE(3)-
TRIGOUT(3)+	17	36	TRIGOUT(3)-
CLKIN(3)+	18	37	CLKIN(3)-
Rsvd	19		

Connection Options:

Cable	Terminal Panel	Description
DNA-CBL-37	DNA-STP-37	DNA-CBL-37 3 foot ribbon cable connects directly to the DNA-STP-37 Screw Terminal Panel.
DNA-CBL-37S	DNA-STP-37	DNA-CBL-37S 3 foot shielded cable connects directly to the DNA-STP-37 Screw Terminal Panel.

Pinout Diagram (serial interface):

Please see the preceding page for counter pinouts.

DB-37 (female) connector

	CHANNEL				*TX Functions*		*RX Functions*	
	0	**1**	**2**	**3**	**TX**	**TX+1***	**RX**	**RX+1***
Pin	4	9	13	18	SER CLK IN+	ACK IN+	SER DATA+	SER CLK IN+
Pin	23	28	32	37	SER CLK IN-	ACK IN-	SER DATA-	SER CLK IN-
Pin	2	7	11	16	EXT TRG IN+	-	FM SYNC IN+	EXT TRG IN+
Pin	21	26	30	35	EXT TRG IN-	-	FM SYNC IN-	EXT TRG IN-
Pin	1	6	10	15	SER DATA+	SER CLK OUT+	SER CLK OUT+	-
Pin	20	25	29	34	SER DATA-	SER CLK OUT-	SER CLK OUT-	-
Pin	3	8	12	17	FM SYN OUT+	-	ACK OUT+	-
Pin	22	27	31	36	FM SYN OUT-	-	ACK OUT-	-

SER CLK = Serial Clock
SER DATA = Serial Data
ACK = Acknowledge
FM SYN = Frame Sync Strobe

*TX+1 and RX+1 signals shown are optional signals. If these signals are to be used, than two channels of the DNx-CT-602-804 board must be committed to each external/user serial port. The base signals of the external serial port will be connected to the DNx-CT-602-804's channel "N" and the optional signals will be connected to board's channel "N+1".

For example, if the ACK IN signal is required, two DNx-CT-602-804 channels will be required to provide all connections required. If channel 0 connections are used for the external port's SER CLK IN, TX SER DATA, etc, than the external port's ACK IN connection will be made to channel 1 pins on the DNx-CT-602-804.