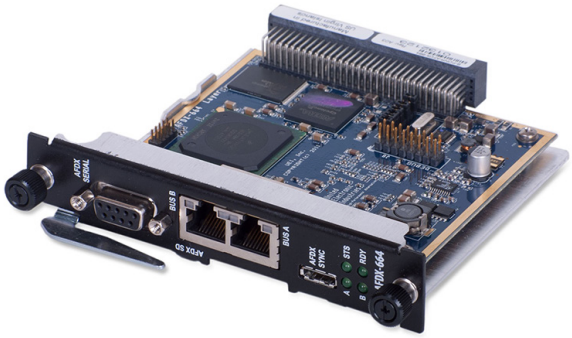
# DNA/DNR-AFDX-664 series

## AFDX / ARINC-664 Interface

- DNA-AFDX-664 for use in "Cube" chassis
- DNR-AFDX-664 for use in RACKtangle® I/O chassis
- 1 dual redundant channels
- 10/100/1000 Base-T implementation
- Transmit, Receive or Bus Monitor function
- Consecutive or user defined Sequence Numbers
- 10 µS, 1 µS and 100 nS time tags
- Error/Integrity checking
- Extensive filtering and traffic scheduling
- Support for Boeing EDE protocol available

10-Year Availability Guarantee



## General Description

The DNA-AFDX-664 and DNR-AFDX-664 are 2 channel AFDX®/ARINC 664 (including the Boeing EDE protocol) communications interfaces for UEI's popular "Cube" and RACKtangle I/O chassis respectively. The boards may be configured as two independent channels or one dual redundant channel. The network implementation fully supports 10, 100 and 1000 BASE-T speeds. The channels may operate as a receiver, transmitter or network/bus monitor.

In input mode, the user may time tag inputs with resolutions as low as 10 microseconds. The input automatically provides error/integrity checking, though this feature may be disabled if the application requires. Receive filtering is also supported based on the VL, Port and error detection.

The Monitor mode allows the user to capture all network traffic, or may be set with automatic filtering so only the desired information is captured. The Monitor mode will also gather a variety of statistics from the bus/network. If desired, the monitor mode may be set to capture all UDP network traffic, regardless of whether it is configured based on the AFDX®/664 protocol.

Transmit channels automatically configure traffic shape via Bandwidth Allocation Gaps (BAG) with 1, 2, 4, 8, 16, 32, 64 or 128 mS timing. Transmission may be based on an automatic scheduler, or in a oneshot asynchronous mode. Both Uni-cast and Multicast are fully supported. The transmitter will automatically generate consecutive Sequence Numbers. All transmission scheduled is done in hardware on-board.

The board is based on the Freescale 8347 processor running the DO-178 certified µC Operating System. In PowerDNA mode, the Cube/RACK itself also uses uC, so though the units are not certified to DO- 178, the fact that the operating system already is will dramatically reduce certification time. Advanced users may also wish to implementspecial functions in the board's firmware which can be implemented with custom µC code. Though the Cube/RACK is well supported with a variety of debugging tools a diagnostic RS-232 port is provided on the board allowing easy access to the lowest levels of the board's functionality.

Software for the DNA/DNR-AFDX-664 series is provided in the UEI Software Suite. A high-level easy to use API is provided for Linux and Linux and more. Windows users may use the UEIDAQ Framework which provides a comprehensive, easy to use API supporting all popular Windows programming languages and applications, including LabVIEW, MATLAB/Simulink and DASYLab as well as any application supporting ActiveX or OPC servers.

## Technical Specifications:

| | |
|---|---|
| **Configuration** | |
| Number of channels | 2: supports A only, B only or dual redundant |
| Ethernet BASE | 10, 100 or 1000 BASE-T |
| Channel functions | Transmit, Receive or Monitor |
| VLs supported | Up to 2000 VLs or ports with up to 664 active |
| Underlying Processor | Freescale 8347 running DO-178 certified OS |
| **Receive Specifications** | |
| Time tagging resolution | 10 µS |
| Error/Integrity checking | Integrity, Link-level, Sequence Number (SN) |
| Filtering | VL, Port and error detection filters |
| **Monitor Specifications** | |
| Configuration | All or Filtered with or without time-tag |
| Error Checking | Capture all, valid or invalid VLs |
| Statistics Gathering | Counters: PHY, Ethernet, IP, UDP, AFDX |
| **Transmit Specifications** | |
| Traffic shape via BAG | 1, 2, 4, 8, 16, 32, 64 or 128 mS |
| Transmission scheduling | 10 µS resolution schedule scheduling of VLs and ports. All scheduling is done in hardware. |
| Transmission configuration | Unicast and multicast addressing |
| Sequence Numbers | Auto-Sequenced Consecutive |
| **General Specifications** | |
| Debugging options | via Cube/RACKtangle chassis backplane or directly to board via RS-232 port. |
| Loop back testing | Loop back mode on the DNx-AFDX-664 allows automatic self-test |
| Operating temperature | tested -40 °C to +85 °C |
| Vibration *IEC 60068-2-6*<br>*EC 60068-2-64* | 5 g, 10-500 Hz, sinusoidal<br>5 g (rms), 10-500 Hz, broad-band random |
| Shock *IEC 60068-2-27* | 50 g, 3 ms half sine, 18 shocks @ 6 orientations<br>30 g, 11 ms half sine, 18 shocks @ 6 orientations<br>30 g, 11 ms half sine, 18 shocks @ 6 orientations |
| Humidity | 5 to 95%, non-condensing |
| Power consumption | 6 Watts, maximum |

## Ordering Guide

| Part Number | Description |
|---|---|
| DNR-AFDX-664 | Dual channel AFDX/ARINC-664 interface for DNR series RACKtangle chassis. |
| DNA-AFDX-664 | Dual channel AFDX/ARINC-664 interface for DNA series CUBE chassis. |

## Block Diagram